Claims

[c1] 1. A mask read-only-memory (ROM) structure, comprising:
a substrate;
a buried bit line embedded inside the substrate;
a patterned stack layer covering a portion of the upper surface of the substrate, wherein the stack layer comprises a first dielectric layer, a stopping layer and a second dielectric layer;
a gate oxide layer covering a portion of the upper surface of the substrate; and
a word line crossing over the buried bit line to form a plurality of coding cells, wherein the coding cells having a stack layer thereon are at a first data state while the coding cells having a gate oxide layer thereon are at a second data state.

[c2] 2. The mask ROM of claim 1, wherein the stack layer includes a first silicon oxide layer, a silicon oxynitride layer and a second silicon oxide layer stacked on top of each other.

[c3] 3. The mask ROM of claim 1, wherein the stack layer includes a first silicon oxide layer, a silicon nitride layer and a second silicon oxide layer stacked on top of each other.

[c4] 4. The mask ROM of claim 1, wherein the first dielectric layer has a thickness between about 200 Å to 800 Å .

[c5] 5. The mask ROM of claim 1, wherein the stopping layer has a thickness between about 20 Å to 80 Å .

[c6] 6. The mask ROM of claim 1, wherein the second dielectric layer has a thickness between about 200 Å to 800 Å .

[c7] 7. A method of manufacturing a mask read-only-memory (ROM), comprising the steps of:
providing a substrate;
forming a first dielectric layer, a stopping layer and a second dielectric layer over the substrate to form a stack layer;
forming a buried bit line in the substrate outside the stack-covered region;

forming a first photoresist layer over the substrate, wherein the first photoresist layer includes a first line/distance pattern;
removing the second dielectric layer and the stopping layer to expose the first dielectric layer using the first photoresist layer as a mask;
removing the first photoresist layer;
forming a second photoresist layer over the substrate, wherein the second photoresist layer includes a second line/distance pattern, and the second line/distance pattern extends in a direction that differs from the direction of extension of the first line/distance pattern;
removing a portion of the second dielectric layer and the first dielectric layer to expose the substrate and the stopping layer using the second photoresist layer and the stopping layer as an etching mask;
forming a gate oxide layer over the exposed substrate; and
forming a word line perpendicular to the direction of extension of the buried bit line to construct a plurality of coding cells, wherein the coding cells having a stack layer thereon are at a first logic state while the coding cells having a gate oxide layer thereon are at a second logic state.

[c8] 8. The method of claim 7, wherein the direction of extension of the first line/distance pattern is perpendicular to the direction of extension of the second line/distance pattern.

[c9] 9. The method of claim 7, wherein the first line/distance pattern in the first photoresist layer includes a plurality of trenches perpendicular to the buried bit line.

[c10] 10. The method of claim 7, wherein the second line/distance pattern in the second photoresist layer includes a plurality of trenches parallel to the buried bit line.

[c11] 11. The method of claim 7, wherein material forming the first dielectric layer and the second dielectric layer includes silicon oxide.

[c12] 12. The method of claim 7, wherein material forming the stopping layer is selected from a group consisting of silicon nitride and silicon oxynitride.

[c13] 13. The method of claim 7, wherein the first dielectric layer has a thickness between about 200 Å to 800 Å .

[c14] 14. The method of claim 7, wherein the stopping layer has a thickness between about 20 Å to 80 Å .

[c15] 15. The method of claim 7, wherein the second dielectric layer has a thickness between about 200 Å to 800 Å .

[c16] 16. The method of claim 7, wherein the step of forming the buried bit line in the substrate includes conducting an ion implantation using the stack layer as an implant mask